IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent Application of:	)	Confirmation No.: 4336
Bunsho Kuramori et al.	)	Examiner: Terry Lee Englund
Application No. 10/670,773	)	Group Art Unit: 2816
Filed: September 26, 2003	)	
For: SUBSTRATE VOLTAGE GENERATING CIRCUIT	)	
	)	July 2, 2007

REPLY BRIEF PURSUANT TO 37 CFR § 41.41

MAIL STOP APPEAL BRIEF- PATENTS
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

This Reply Brief is submitted in response to the Examiner's Answer dated April 30, 2007.

In setting forth the rejection of claims 1-6 under 35 U.S.C. § 112, first paragraph, at page 4 of the Examiner's Answer, the Examiner asserts, "The circuit (as shown in Fig. 1), and as claimed in claim 1, would not be able to generate a third potential level (e.g., VBB) lower than the second potential level (e.g., VSS). Therefore, what apparently generates the third potential level, and applies it to node OUT_vbb, is not shown, disclosed, or claimed." Additionally, at page 7, in the "Response to Argument" section of the Answer, the Examiner asserts, "Until the applicants can clearly describe how the output node of the present invention can have a third potential level (e.g., VBB) lower than the second potential level (e.g., VSS) as cited within independent claim 1, the rejections of claims 1-6 described in the previous Office Action, and within this Examiner's Answer, will be maintained." While Appellants believe sufficient explanation was provided in the Amendment After Final filed

on May 30, 2006[1] (see, pages 9-10), and in the Brief (see, pages 10-11), Appellants respectfully submit the following additional and more detailed explanation of the output side of the substrate voltage generating circuit shown in FIG. 1 for the Examiner's consideration:

1) Node n1 is charged from a voltage VSS to a voltage VBB by temporarily lowering down a voltage potential of the node n1 based on a charging of capacitor C1 being supplied with a voltage VSS to the depicted left hand terminal of the capacitor. At this time, the output terminal OUT_vbb is supplied the temporarily lowered voltage of the node n1 (i.e., VBB) by the switch SW1 being in a conductive state.

2) Similarly, node n2 is charged from a voltage VSS to a voltage VBB by temporarily lowering down a voltage potential of the node n2 based on a charging of capacitor C2 being supplied with a voltage VSS to the depicted left hand terminal of the capacitor. At this time, the output terminal OUT_vbb is supplied the temporarily lowered voltage of the node n2 (i.e., VBB) by the switch SW2 being in a conductive state.

The voltage VBB generates at the output by alternating the above operations 1) and 2).

In FIG. 1, the Examiner correctly notes that node n1 is directly connected to a node supplied with the voltage VSS and that the node n2 is directly connected to a node supplied with the voltage VSS. However, the output terminal OUT_vbb keeps the voltage VBB by the switch SW1 being switched to a non-conductive state before the node n1 goes from the temporarily lowered voltage VBB to the voltage VSS while switching the switch SW2 to a conductive state, and by the switch SW2 switching to a non-conductive state before the node n2 goes from the temporarily lowered voltage VBB to the voltage VSS while switching the switch SW1 to a conductive state. Accordingly, the circuit shown in FIG. 1 generates the voltage VBB at the output terminal OUT_vbb.

---

[1] Upon further review of the most recently submitted Appeal Brief, Appellants noted an error in the Section IV: Status of Amendments. In that section, Appellants failed to state that the Examiner had considered the Amendment After Final would enter the Amendment After Final for the purposes of appeal, as indicated in the Advisory Action mailed on July 5, 2006, in items 7 and 11. However, it is not clear whether the amendment to the title of the invention was entered because the PTO PAIRS database includes an image of the first page of the Amendment After Final that indicates the amendment was not entered.

Contrary to the Examiner's assertions, claim 1 recites such a voltage VBB, namely, "an output node having a third potential level lower than the second potential level," and Appellants' disclosure includes at least one exemplary way to achieve such a third potential level that would have been sufficient for one of ordinary skill in the art to carry out the invention without undue experimentation. Furthermore, Appellants submit that one of ordinary skill in the art would appreciate the phenomena of a temporary lowered potential at each node n1 and n2 after capacitors c1 and c2 respectively having one terminal connected to these nodes are switched, as explained above. Accordingly, Appellants respectfully submit that claims 1-6 are fully enabled by the original disclosure.

In light of the foregoing, and the arguments presented on pages 8 to 14 of the amended Appeal Brief filed on December 15, 2006, it is respectfully submitted that the Examiner's rejections of claims 1-10 under Section 112, first and second paragraphs, are erroneous and should be reversed.

Respectfully submitted,

/John F. Guay, Reg.# 47248/
John F. Guay

NIXON PEABODY LLP
401 Ninth Street, N.W.
Suite 900
Washington, D.C. 20004